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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,277	11/09/2001	Donald M. Bartlett	LSI.08USC1 (95-133/1P/1C/	3839

24319 7590 09/27/2002

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n N .	Applicant(s)	
	09/991,277	BARTLETT ET AL.	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Pap r No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the preliminary amendment filed February 2, 2002.

Drawings

Figure 1 should be designated by a legend such as --**Prior Art**-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-7 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figure 1 in view of Sogo et al. (US 2002/0027244 A1) and Dakshina-Murthy (US 6,406,950 B1).

Prior Art Figure 1 teaches an integrated circuit having a plurality of circuits **10** & **30** formed on a common substrate **15** and circuitry formed on predetermined portions of the common substrate. However, Prior Art Figure 1 fail to teach masking predetermined

locations of a common substrate that are aligned with the isolation region; and irradiating the common substrate with the high energy ions such that the high energy ions have an energy level sufficient to implant the high energy ions in embedded regions of the common substrate. Sogo et al. teaches masking predetermined locations of a common substrate **4** that are aligned with a material capable of masking high energy ions and irradiating the common substrate with the high energy ions such that the high energy ions have an energy level sufficient to implant the high energy ions in embedded regions of the common substrate that have a lower resistance than the common substrate; boron and phosphorus ions; a checkerboard patter of embedded regions; and irradiating a wafer with ions in the range of approximately 1 to 2 MeV (Figures 10A-10B & 12B, page 2, paragraps [0012]-[0013]). Dakshina-Murthy teaches masking predetermined locations of a common substrate **12** that are aligned with the isolation region **18** and isolation regions having a higher resistance than the common substrate are formed in the common substrate between the embedded region **42** & **64** and the embedded regions are buried in the common substrate so that the currents injected into the common substrate by the circuits preferentially flow to a ground potential rather than through the isolation region (Figure 14, col. 7, lines 26-51). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify forming the integrated circuit of Prior Art Figure 1 with the high energy ions of Sogo et al. and the isolation region of Dakshina-Murthy to obtain a low power dissipating integrated circuit.

Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figure 1, Sogo et al. (US 2002/0027244 A1) and Dakshina-Murthy (US 6,406,950 B1) as applied to claims 1-2, 4-7 and 9-11 above, and further in view of Diaz (5,760,445).

Prior Art Figure 1, Sogo et al. and Dakshina-Murthy teach all mentioned in the rejection above. However, Prior Art Figure 1, Sogo et al. and Dakshina-Murthy fail to teach a substrate including an epitaxial layer and an underlying substrate layer. Diaz teaches a substrate including an epitaxial layer **226** and an underlying substrate layer **228** (Figures 2A-2C, cols. 4-5, lines 62-67 and 1-10, respectively). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify forming the integrated circuit of Prior Art Figure 1, the high energy ions of Sogo et al. and the isolation region of Dakshina-Murthy with the substrate of Diaz to eliminate degradation to device characteristics.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to high energy implanted structures:

Hshieh (US 6,426,260 B1)

Hu et al. (H707)

Matukura et al. (3,582,725)

Worley (6,020,614).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims
September 18, 2002

Carl Whitehead Jr.
CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800